CLAIMS

1. A method for forming an interconnection between a storage capacitor and a transfer device in a memory cell, the method comprising the steps of:

a) forming a capacitor having a lip extending over a top surface of a substrate; and

b) diffusing dopant from the lip into the top surface of the substrate.

2. The method of claim 1 wherein the step of forming a capacitor having a lip extending over a top surface of a substrate comprises:

i) forming a first layer on the substrate;

ii) etching an oversized capacitor opening in the first layer;

iii) forming a sidewall spacer on sidewall of the oversized capacitor opening;

iv) etching a trench in the substrate using the sidewall spacer as a mask;

v) removing the sidewall spacer; and

vi) filling the trench and oversized capacitor opening with capacitor fill material.

3. The method of claim 2 wherein the capacitor fill material comprises polysilicon.

4. The method of claim 2 wherein the step of forming a capacitor having a lip extending over a top surface of a substrate further comprises:

vii) recessing the capacitor fill material partially into the oversized capacitor opening; and

viii) filling the recess in the oversized capacitor opening with a dielectric material.

5. The method of claim 1 wherein the step of diffusing dopant from the lip into the top surface comprises annealing the substrate and the capacitor.

6. The method of claim 1 wherein the first layer comprises a gate stack including:

i) a gate dielectric layer;

ii) a gate conductor layer on the gate dielectric layer; and

iii) an insulator layer on the gate conductor layer.

7. The method of claim 6 wherein the gate conductor layer comprises polysilicon.

8. The method of claim 6 wherein the insulator layer comprises a layer of silicon nitride and a layer of silicon dioxide.

9. The method of claim 1 wherein the first layer comprises a layer of silicon dioxide, a layer of silicon nitride, and an a layer of silicon dioxide.

10. The method of claim 1 wherein the step of forming a capacitor comprises the steps of:

i) forming a gate stack, the gate stack including a gate dielectric, a gate conductor on the gate dielectric, and an insulator layer on the gate conductor;

ii) etching an oversized capacitor opening in the gate stack;

iii) forming a sidewall spacer on sidewall of the oversized capacitor opening;

iv) etching a trench in the substrate using the sidewall spacer and the insulator layer on the gate conductor as a mask;

v) removing the sidewall spacer;

vi) forming an oxide collar in the trench;

vii) filling the trench and oversized capacitor opening with a capacitor fill material thereby forming a lip of capacitor fill material at the top of the trench;

viii) recessing the capacitor fill material partially into the oversized capacitor opening;

ix) filling the recess in the oversized capacitor opening with a dielectric material; and

x) forming shallow trench isolation, the shallow trench isolation removing portions of the lip except where a connection from the capacitor to the transfer device is to be formed.

11. The method of claim 10 further comprising the steps of:

d) patterning the remaining gate conductor stack; and

e) forming sidewall spacers on the sidewalls of the patterned gate conductor stack.

12. The method of claim 1 wherein the step of forming a capacitor comprises the steps of:

i) forming a gate stack, the gate stack including a gate dielectric, a gate conductor on the gate dielectric, and an insulator layer on the gate conductor;

ii) etching an oversized capacitor opening in the gate stack;

iii) forming a sidewall spacer on sidewall of the oversized capacitor opening;

iv) etching a trench in the substrate using the sidewall spacer and the insulator layer on the gate conductor as a mask;

v) removing the sidewall spacer;

vi) forming an oxide collar in the trench;

vii) filling the trench and oversized capacitor opening with a capacitor fill material thereby forming a lip of capacitor fill material at the top of the trench;

viii) recessing the capacitor fill material partially into the oversized capacitor opening;

ix) filling the recess in the oversized capacitor opening with a dielectric material;

Claim 12 continued:

x) forming shallow trench isolation, the shallow trench isolation removing portions of the gate stack and portions of the capacitor lip except where a connection from the capacitor to the transfer device is to be formed;

xi) planarizing shallow trench isolation and the remaining gate stack, such that a portion of the insulator layer remains on the gate conductor layer;

xii) removing a portion of the remaining insulator layer between shallow trench isolation regions, the removal exposing portions of the underlying gate conductor material;

xiii) depositing wordline line material that contacts the exposed gate conductor material;

xiv) patterning the wordline and gate conductor material to form a plurality of gates;

xv) forming a source/drain implants; and

wherein the step of diffusing dopant from the lip into the top surface of the substrate comprises annealing, and wherein the dopant diffused from the lip to the top surface comprises a source/drain of the transfer device and wherein the source/drain implant diffuses to form a source/drain of the transfer device.

13. The method of claim 12 wherein the step of patterning the wordline and gate conductor material comprises etching selective to the remaining insulator material to avoid etching the gate conductor material at portions adjacent to the capacitor.

14. The method of claim 12 wherein the step of removing a portion of the remaining insulator layer between shallow trench isolation regions comprises leaving a portion extending into area where the gate will be formed to compensate for potential alignment errors.

15. The method of claim 1 wherein the step of forming a capacitor comprises the steps of:

i) forming a first layer on the substrate, the first layer comprising a first silicon dioxide layer, a silicon nitride layer and second silicon dioxide layer;

ii) etching an oversized capacitor opening in the first layer;

iii) forming a sidewall spacer on sidewall of the oversized capacitor opening;

iv) etching a trench in the substrate using the sidewall spacer and the first layer as a mask;

v) removing the sidewall spacer;

vi) forming an oxide collar in the trench;

vii) filling the trench and oversized capacitor opening with a capacitor fill material thereby forming a lip of capacitor fill material at the top of the trench;

viii) recessing the capacitor fill material partially into the oversized capacitor opening;

ix) filling the recess in the oversized capacitor opening with a dielectric material;

x) forming shallow trench isolation, the shallow trench isolation removing portions of the lip except where a connection from the capacitor to the transfer device is to be formed.

16. The method of claim 12 further comprising the steps of:

c) removing remaining portions of the first layer;

d) forming gate dielectric;

e) depositing a gate conductor material;

f) patterning the gate conductor.

17. A method for forming a connection between a capacitor and a transfer device on a semiconductor substrate having a top surface, the method comprising the steps of:

a) forming a first layer on the semiconductor substrate;

b) etching an oversized capacitor opening in the first layer;

c) forming a sidewall spacer on the sidewalls of the oversized capacitor opening;

d) etching a capacitor trench in the semiconductor substrate using said sidewall spacer and said first layer as a mask, said capacitor trench having a top edge at the top surface of said semiconductor substrate;

e) depositing capacitor fill material in said capacitor trench, said capacitor fill material extending over said capacitor trench top edge to form a lip of capacitor fill material on said top surface of said semiconductor substrate; and

f) diffusing dopants from said capacitor fill material into said semiconductor substrate from said lip of capacitor fill material.

18. The method of claim 17 wherein the first layer comprises a gate dielectric layer, a gate conductor layer and a insulator layer.

19. The method of claim 17 wherein the first layer comprises a first silicon dioxide layer, a silicon nitride layer and second silicon dioxide layer.

20. The method of claim 17 wherein the step of depositing capacitor fill material comprises performing a first deposition of capacitor fill material, recessing said first deposition of capacitor fill material, said recess partially exposing sidewalls of said capacitor trench, forming sidewall spacers on said exposed sidewalls of said capacitor trench, and refilling the capacitor trench and oversized capacitor opening.

21. The method of claim 17 wherein the capacitor fill material comprises n+ doped polysilicon.

22. The method of claim 17 wherein the step of diffusing dopants from said capacitor fill material into said semiconductor substrate from said lip of capacitor fill material comprises annealing the semiconductor substrate.

23. The method of claim 17 further comprising the step of etching an isolation trench, wherein said etching of said isolation trench removes a portion on said lip of capacitor fill material except where a connection between said capacitor and said transfer device is to be made.

24. The method of claim 23 further comprising the step of filling said isolation trench with isolation material and planarizing said isolation material.

25. The method of claim 24 wherein the first layer comprises a gate dielectric layer, a gate conductor layer and a insulator layer and wherein the step of planarizing said isolation material removes said insulator layer to expose said gate conductor material.

26. The method of claim 24 wherein the first layer comprises a gate dielectric layer, a gate conductor layer and a insulator layer and wherein the step of planarizing said isolation material leaves a portion of the insulator layer covering the gate conductor layer.

27. The method of claim 25 further comprising the step of depositing a wordline material layer on said gate conductor material and said isolation material, and further comprising the step of patterning the gate conductor material and wordline material to form a plurality of transfer device gates.

28. The method of claim 26 further comprising the steps of etching an opening in the remaining portion of the insulator layer to expose a portion of the gate conductor layer and depositing a wordline material layer on the exposed gate conductor material, the remaining insulator layer and the isolation material, and further comprising the step of patterning the gate conductor material and wordline material to form a plurality of transfer device gates, wherein the remaining insulator layer serves as an etch block to prevent unwanted etching of the gate conductor material.

29. The method of claim 24 wherein the first layer comprises a first silicon dioxide layer, a silicon nitride layer and second silicon dioxide layer wherein the step of planarizing said isolation material removes any remaining portion of said second silicon dioxide layer and planarizes said silicon nitride layer, and further comprising the step of removing said silicon nitride layer and forming a gate dielectric layer, a gate conductor layer, and a wordline material layer, and further comprising the step of pattering said gate dielectric layer, said gate conductor layer and said wordline material layer to define a gate of the transfer device.

30. An apparatus for connecting a capacitor to a transfer device in a memory cell formed on a substrate, the apparatus comprising dopant diffused from a capacitor lip formed at the top of the capacitor, the capacitor lip extending over and contacting the top surface of the substrate.

31. The apparatus of claim 30 wherein the capacitor lip extends between 1 nm and 200 nm.

32. The apparatus of claim 30 wherein the capacitor lip extends between 10 nm and 50 nm.

33. The apparatus of claim 30 wherein the dopant diffuses in a substantially vertical direction.

34. The apparatus of claim 30 further comprising a layer of insulating material covering the capacitor lip.

35. The apparatus of claim 30 wherein said diffused dopant contacts capacitor sidewalls less than one half the depth of an adjacent source/drain of the transfer device.

36. The apparatus of claim 30 wherein said capacitor comprises n+ doped polysilicon, and wherein said dopant is diffused from said n+ doped polysilicon.

37. The apparatus of claim 30 wherein said diffused dopant comprises a source/drain for the transfer device.

38. The apparatus of claim 30 wherein said diffused dopant is adjacent to and contacts a source/drain of the transfer device.

39. The apparatus of claim 30 wherein said diffused dopant has a depth at most approximately equal to the depth of an adjacent source/drain of the transfer device.

40. The apparatus of claim 30 wherein portions of said lip are removed by an isolation region trench.

41. The apparatus of claim 30 wherein said diffused dopant is self aligned with the capacitor.

42. The apparatus of claim 30 further comprising an isolation collar at the top of said capacitor, said isolation collar isolating sidewalls of said capacitor from adjacent portions of a silicon substrate.

43. A memory cell formed on a substrate, the memory cell comprising:

a) a transfer device having a source/drain;

b) a trench capacitor, the trench capacitor having a lip of capacitor fill material extending over the top surface of the substrate;

c) an isolation trench formed in said substrate, said isolation trench removing portions of said lip of capacitor fill material while leaving said lip of capacitor fill material adjacent to said transfer device;

d) an isolation collar at the top of said trench capacitor, said isolation collar isolating said trench capacitor from adjacent portions of said substrate; and

e) a surface strap comprising dopant diffused from the lip of capacitor fill material, the surface strap being self aligned with the trench capacitor.

44. The apparatus of claim 43 wherein said substrate comprises a silicon wafer and wherein said capacitor fill material comprises n+ doped polysilicon.

45. The apparatus of claim 43 wherein said surface strap has a depth less at most approximately equal to the to the depth of an adjacent source/drain of the transfer device.

*****